Inventor (s): Kellerman et al.

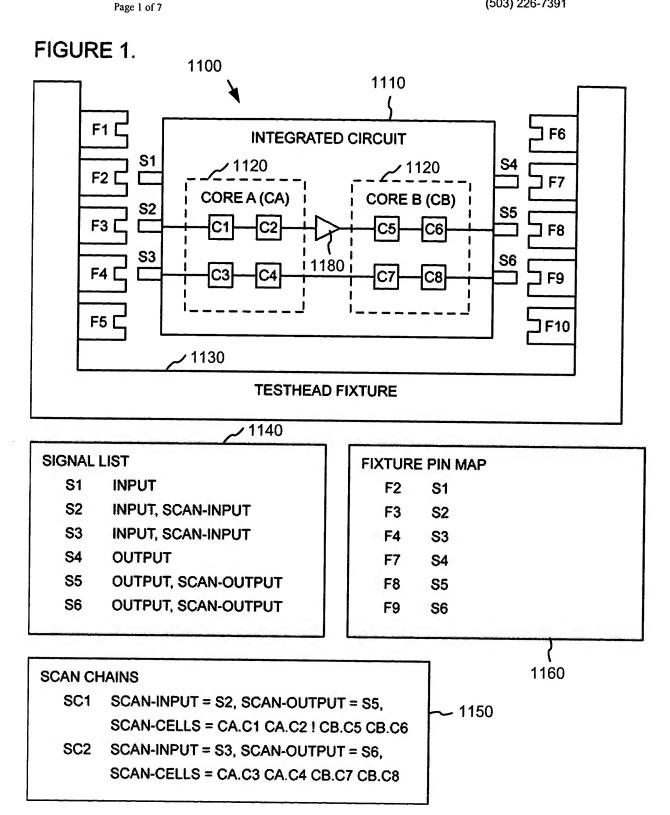
Date of Deposit: June 19, 2003

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Title: CREATION, VIEWING, AND ANALYSIS OF THE RESULTS OF INTEGRATED CIRCUIT TEST PROGRAMS CONSISTING OF SCAN TESTS

Attorney Matter No.: 6769-65390/SAW

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FIGURE 2.

	\ <u>_</u>	••	1200 مر
			SULT VECTORS AND SIGNALS)
	TEST 1 SETUP	RESULTS	TEST 2 SETUP RESULTS
S1	0	-	1 -
S2	1	-	0 -
S3	0	-	1 -
S4	-	1	- 1
S 5	-	1	- 0
S6	-	0	- 1
C1	0	1	1 0
C2	1	0	1 1
C3	0	0	0 0
C4	0	1	0 1
C5	1	0	1 0
C6	1	1	1 1
C7	0	1	0 0
C8	1	0	0 1

1210 سر

TEST PROGRAM, NO TEST OVERLAP							
TEST 1:							
SHIFT	S2 = 0010, S3 = 1000						
CYCLE	S1 = 0, S2 = 1, S3 = 0						
CYCLE	S4 = H, S5 = H, S6 = L						
SHIFT	S5 = HLHL, S6 = LHHL						
TEST 2:							
SHIFT	S2 = 0011, S3 = 0000						
CYCLE	S1 = 1, S2 = 0, S3 = 1						
CYCLE	S4 = H, S5 = L, S6 = H						
SHIFT	S5 = HLLH, S6 = HLHL						

1 0	TEST PROG	RAM, LOAD/UNLOAD OVERLAP	
1 1	TEST 1: SHIFT	S2 = 0010, S3 = 1000	
) 1	CYCLE CYCLE TEST 2:	S1 = 0, S2 = 1, S3 = 0 S4 = H, S5 = H, S6 = L	
1220 ~	SHIFT CYCLE CYCLE SHIFT		

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FIGURE 3.

	1300 مر															
CYCLIZED TEST PROGRAM																
	CYCLE															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
S1	-	-	-	-	10	l -] -	-	-	-	11	 -] -	-	-	
S2	0	0	1	0	11	<u> </u> _	¦ο	0	1	1	0	<u> </u>	ļ _	-	-	_
S3	1	0	0	0	ļo	j.	0	0	0	0	1	į.	i _	-	-	•
S4	į-	-	-	-	i -	Н	-1	-	-	-	 -	Н	 -	-	-	-
S5] -	-	-	-	-	Н	Н	L	Н	L	! -	L	l I H	L	L	Н
S6	-	-	-	-	-	L	L	Н	Н	L	 -	Н	Н	L	Н	L
	TEST 1 LOAD				TEST 1 LAUNCH	TEST 1 CAPTURE	TEST 1 UNLOAD /	TEST 2 LOAD			TEST 2 LAUNCH	TEST 2 CAPTURE	TEST 2 UNLOAD			

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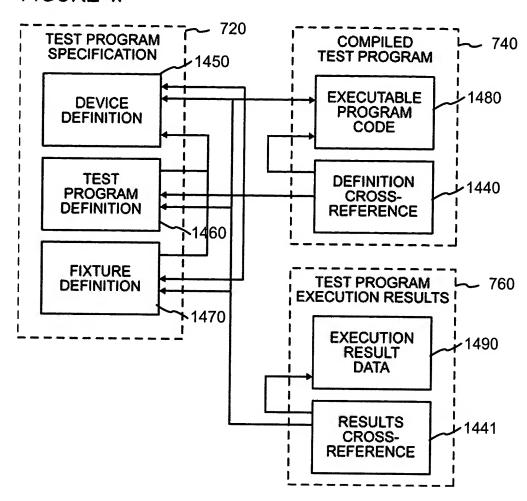
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FIGURE 4.



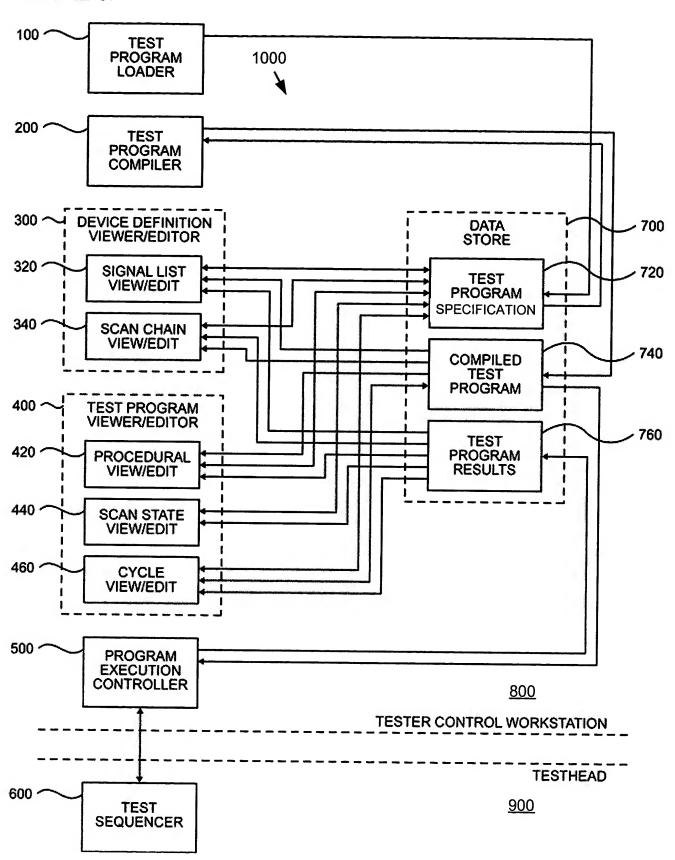
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FIGURE 5.



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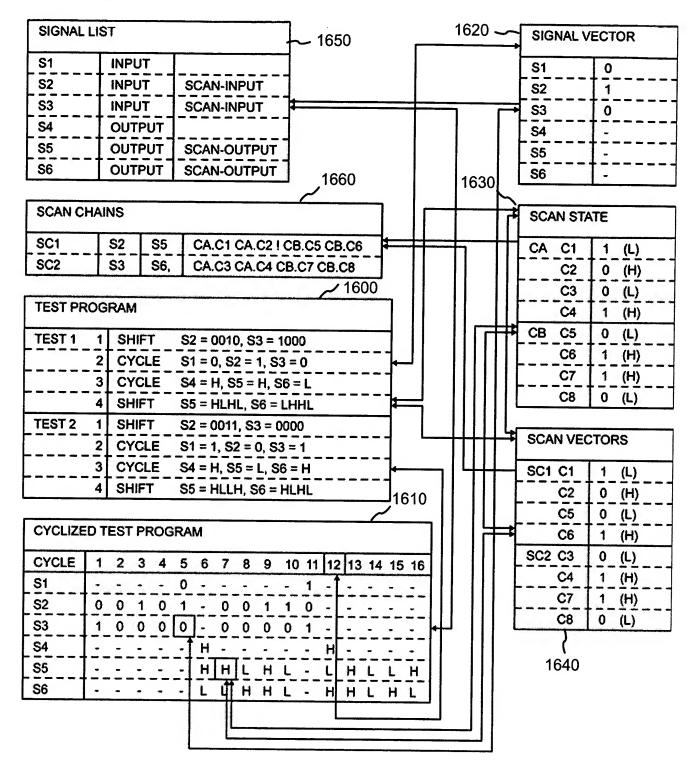
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FIGURE 6.



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FIGURE 7.

